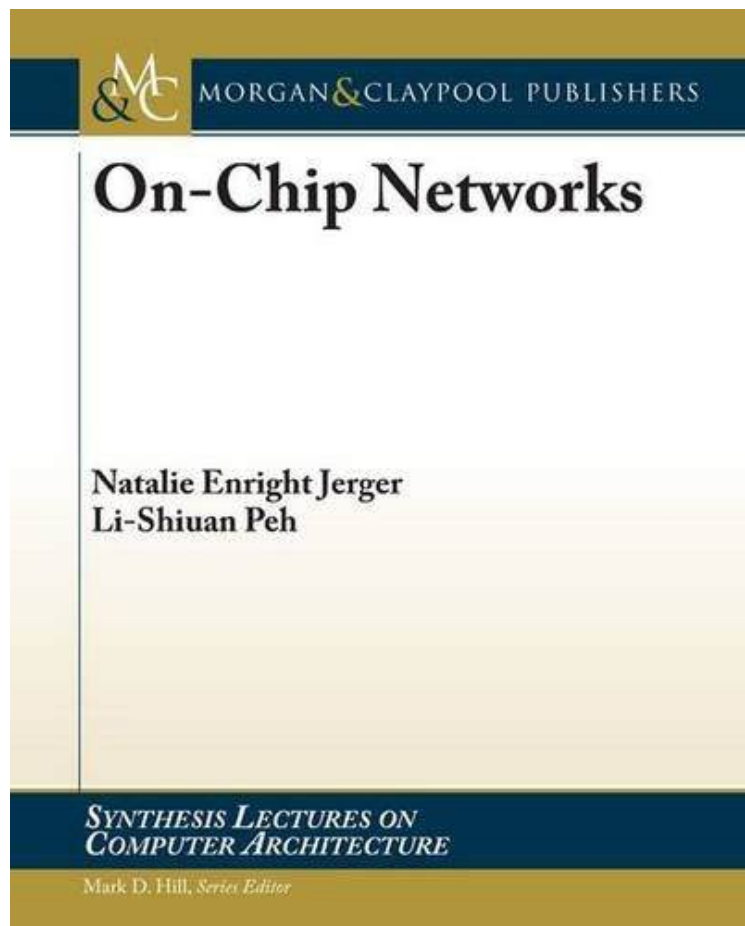


# On-Chip Networks (Synthesis Lectures on Computer Architecture)

By Li-Shiuan Peh, Natalie Enright Jerger



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With the ability to integrate a large number of cores on a single chip research into on chip networks to facilitate communication becomes increasingly important On chip networks seek to provide a scalable and high bandwidth communication substrate for multi core and many core architectures High bandwidth and low latency within the on chip network must be achieved while fitting within tight area and power budgets In this lecture we examine various

fundamental aspects

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